REMARKS

Claims 3, 4, 6-9, 11-17, 19-26, 55-62 and 75-79 are pending in this application. Applicant acknowledges, with appreciation, the Examiner's allowance of claims 8, 9, 11, 12, 15-17, 22-26, 55-62 and 75-78. In this Amendment, claims 3, 4, 6-9, 11-15, 19, 22, 25, 26, 78 and 79 have been amended only for clarification. Care has been exercised to avoid the introduction of new matter. The specification and drawings have also been amended.

Claim Objections

The Examiner stated that claims 3, 4, 6-9, 11-15, 19, 22, 25, 26, 78 and 79 should be amended to replace the term "clock signal" with --output clock signal--. In response, Applicant has amended the claims in a manner suggested by the Examiner. Withdrawal of the objection to the claims is respectfully solicited.

Drawings

The Examiner asserted that the limitations recited in claims 13 and 14 are not shown in the drawings. In response, Fig. 2 has been amended to illustrate what is recited in claims 13 and 14. No new matter has been added. Relevant description of claims 13 and 14 can be found in, for example, the paragraphs on page 18, lines 2-19 of the specification, which have also been amended in relation to the amendment of Fig. 2. Applicant believes that the amendment of Fig. 2 is fully responsive to the Examiner's concerns, and respectfully solicits withdrawal of the objection to the drawings.

In addition, Applicant explains Fig. 2 in more detail. The duty ratio of the output buffer signal can be adjusted using control signals P11-P1n and N11-N1n by adjusting the amount of change in power supply potential VCC or ground potential GND using control signals P11-P1n, N11-N1n, respectively.

The power supply potential VCC or ground potential GND can be supplied by another power supply source or ground source using control signals P11-P1n, N11-N1n, respectively. The power supply potential VCC or ground potential GND can also be generated by up-converting or down-converting another power supply potential or ground potential using control signals P11-P1n, N11-N1n, respectively. The power supply potential VCC or ground potential GND can also be supplied by switching the power supply potential or ground potential with the voltage control function of a regular circuit using control signals P11-P1n, N11-N1n, respectively.

The duty ratio of the output buffer signal can be adjusted using control signals P21-P2n and N21-N2n by adjusting the amount of change in substrate potential of the transistor using control signals P21-P2n and N21-N2n.

The substrate potential of the transistor can be supplied by another transistor using control signals P21-P2n and N21-N2n. The substrate potential of the transistor can also be generated by up-converting or down-converting another substrate potential using control signals P21-P2n and N21-N2n. The substrate potential of the transistor can also be supplied by switching the substrate potential with the voltage control function of a regular circuit using control signals P21-P2n and N21-N2n.

Claims 3, 4, 13 and 14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yen of record in view of Applicant Admitted Prior Art ("AAPA")

With respect to claim 3, the Examiner admitted that Yen does not teach the following limitations: "at least one of a power supply potential or a ground potential in said buffer circuit is different from another power supply voltage or ground voltage, respectively, in said buffering portion." Then, the Examiner applied Applicant's arguments as AAPA, and asserted that AAPA teaches the above limitation. This rejection is respectfully traversed.

First, the Examiner did not provide any support for respective claims 3, 4, 13 and 14 that AAPA teaches the limitations recited in those claims. The Examiner is required to consider whether AAPA teaches the claimed invention by comparing the actually recited claim limitations in each claim with AAPA.

Applicant invites the Examiner's attention to the arguments on page 22, the first full paragraph of the September 7, 2005 reply. In the reply, it is specifically noted that the conventional technologies discussed are employed to control the power supply/ground potential in a whole LSI or a large module unit. The object of the conventional technologies is either to lower the power supply voltage or to raise the threshold voltage. In contrast, the claimed invention is configured to control specific gates, thereby controlling the duty ratio of a clock signal. The conventional technologies do not teach the claimed limitation. Applicant respectfully requests the Examiner to consider the above Applicant's comments.

Second, there is no motivation to modify Yen's circuit based on AAPA to arrive at the claimed invention. In imposing a rejection under 35 U.S.C. §103, the Examiner is required to make a "thorough and searching" factual inquiry and, based upon such a factual inquiry, explain why one having ordinary skill in the art would have been realistically impelled to modify particular prior art, in this case Yen's circuit, to arrive at the claimed invention. *In re Lee*, 277 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). Merely identifying features of a claimed invention in disparate prior art references does not, automatically, establish the requisite motivation for combining references in any particular manner. *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999); *Grain Processing Corp. v. American-Maize Products Co.*, 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).

The Examiner's asserted motivation to modify Yen's circuit is that "such configuration would provide potential control versatility as taught by the Applicant Admitted Prior Art" (see page 5, the first full paragraph of the Office Action). However, this assertion does not provide any reason why a person skilled in the art would have been motivated to modify Yen to arrive at the claimed invention.

The AAPA (Applicant's argument cited by the Examiner) does not teach that "such configuration would provide potential control versatility" for a buffer circuit of a clock generation circuit. As mentioned above, what Applicant's arguments teach is that the conventional technologies discussed are employed to control the power supply/ground potential in a whole LSI or a large module unit. Accordingly, the Examiner's assertion does not specifically address the claimed invention, and is not enough to conclude that there is support to modify Yen's circuit to arrive at the claimed invention. The Examiner is required to show facts. *See In re Lee*, supra.

Based upon the foregoing, Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention for lack of the requisite factual basis and want of the requisite realistic motivation. Applicant, therefore, submits that the imposed rejection of claims 3, 4, 13 and 14 under 35 U.S.C. §103 for obviousness predicated upon Yen in view of AAPA is not factually or legally viable and, hence, respectfully solicits withdrawal thereof.

Claims 6, 19-21 and 79 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yen in view of Yamaguchi et al.

In the statement of the rejection, the Examiner admitted that Yen fails to teach, among other things, the counter and the control circuit recited in independent claims 6, 19 and 79. However, the Examiner applied Yamaguchi et al. and asserted that the reference teaches the missing features of Yen. This response is respectfully traversed because Yamaguchi et al. does not teach, among other things, the counter and the control circuit recited in the independent claims.

The Examiner asserted that up-and-down counter 43 and stage number controller 44 in Fig. 4 of Yamaguchi et al. correspond to the claimed counter and control circuit. Yamaguchi et al. states that up-and-down counter 43 produces counting signals C1 through Ch. Stage number controller 44 receives the counting signals C1-Ch from up-and down counter 43 to produce activating signals S1-Sg to oscillator 45. See column 5, lines 15-21 of Yamaguchi et al. Stage number controller controls oscillator 45 in Yamaguchi et al.

In contrast, the claimed control circuit is configured to increment/decrement a digital count value of the claimed counter. The counter is configured to determine the digital count value set by the control circuit based on a phase comparison result. The claimed control circuit does not receive the digital count value from the counter to produce activating signals for the ring oscillator. Unlike Yamaguchi's circuit, the claimed control circuit does not directly control the oscillator.

Based upon the foregoing, Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention for lack of the requisite factual basis. Applicant, therefore, submits that the imposed rejection of claims 6, 19-21 and 79 under 35 U.S.C. §103 for obviousness predicated upon Yen in view of Yamaguchi et al. is not factually or legally viable and, hence, respectfully solicits withdrawal thereof.

Claim 7 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Yen in view of Suda.

In the statement of the rejection, the Examiner admitted that Yen fails to teach the frequency-multiplied circuit and the ring oscillator, recited in claim 7. The Examiner applied Suda and asserted that the reference teaches those missing features. Then, the Examiner concluded that it would have been obvious to modify Yen's device based on the teachings of Suda to arrive at the claimed invention.

Applicant specifically submits that the applied combination does not teach, among other things, the ring oscillator including the selector selecting and outputting an input from one of the first and second delay line.

The Examiner asserted that selector 116 of Suda (Fig. 16) corresponds to the claimed selector. Selector 116 in Suda is a portion of the delay line and is required to constitute the delay line. In contrast, the claimed selector does not constitute the delay line, but selects and outputs an input from one of the first and second delay line, as claimed.

For example, it may be said that delay lines 74, 75 in Fig. 17 of the application include the function of selector 116 in Suda. There are many circuit topologies to implement the function of delay lines 74, 75. If the circuit topologies described in Suda were adapted to delay lines 74, 75 in Fig. 17 of the application, delay lines 74, 75 would include a circuit component like selector 118 of Suda. That component cannot be removed from the delay lines 74, 75 because the component is part of the delay lines and is required for the operation of the delay lines. If selector 116 were removed from the delay line of Suda, the delay line would become no longer a delay line, but a buffer circuit that totally loses the function to control the clock phase. In contrast, the claimed invention maintains the function of clock generation circuit even if the selector (e.g., selector 77 in Fig. 17 of the application) is removed.

From another point of view, if delay line 74, 75 in Fig. 17 of the present application were to adapt the circuit mentioned in Suda, a selector would have to be added to the output portions of delay lines 74, 75 as shown in Fig. 16 of Suda, in addition to selector 77 of Fig. 17 of the application. This would add require another selector in the claimed invention (former and latter selectors). The former selector is the selector disclosed in Suda, while the latter selector is not disclosed in Suda. The latter selector would correspond to the selector in claim 7. A person of ordinary skill in the art would not have been led to such a modification from the reference teachings.

Based upon the foregoing, Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention for lack of the requisite factual basis. Applicant, therefore, submits that the imposed rejection of claim 7 under 35 U.S.C. §103 for obviousness predicated upon Yen in view of Suda not factually or legally viable and, hence, respectfully solicits withdrawal thereof.

Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Amendments to the Drawings

The attached sheet of drawings includes changes to Fig. 2. This sheet, which includes Figs. 1-3, replaces the original sheet including Figs. 1-3. In Fig. 2, control signals P11-P1n, P21-P2n, N11-N1n and N21-N2n are added.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

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FIG.1

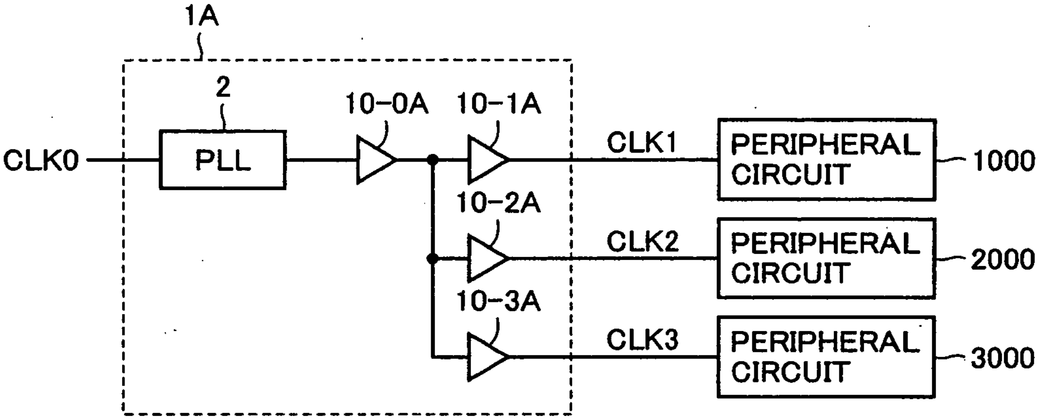
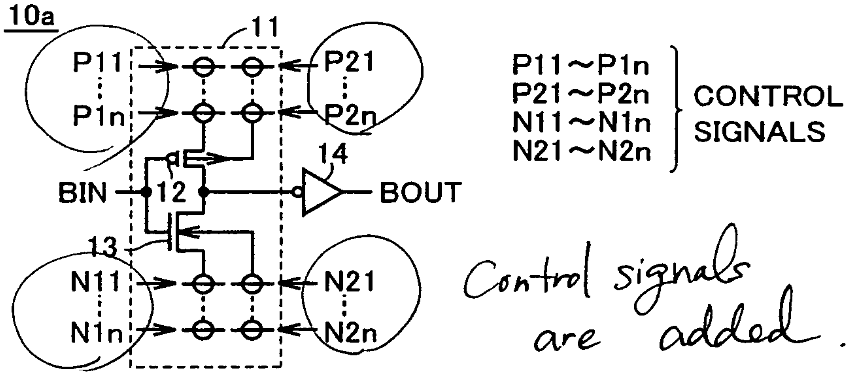


FIG.2



Control signals are added.

FIG.3